selection lines GSL and SSL, eight word lines WL**1** to WL**8**, and three bit lines BL**1** to BL**3**, but the number of the lines may be variously changed.

[0091] The substrate SUB may have a first conductive type (for example, a p type), and a common source line CSL that extends along the first direction (for example, a Y direction), and is doped with impurities having a second conductive type (for example, an n type) may be provided on the substrate SUB. A plurality of insulation layers IL that extend along the first direction may be sequentially provided along the third direction (for example, a Z direction) in a region of the substrate SUB between two adjacent common source lines CSL, and may be spaced apart from each other along the third direction. For example, the plurality of insulation layers IL may each include an insulating material such as silicon oxide and/or the like.

[0092] A plurality of pillars P, which are sequentially arranged along the first direction and pass through the plurality of insulation layers IL along the third direction, may be provided in a region of the substrate SUB between two adjacent common source lines CSL. For example, the plurality of pillars P may contact the substrate SUB through the plurality of insulation layers IL, In an example embodiment, a surface layer S of each of the pillars P may include silicon having a first type and may function as a channel region. Also, an inner layer I of each of the pillars P may include an insulating material, such as silicon oxide and/or the like, or an air gap.

[0093] A charge storage layer CS may be provided along the insulation layers IL, the pillars P. and an exposed surface of the substrate SUB and in a region of the substrate SUB between two adjacent common source lines CSL. The charge storage layer CS may include a gate insulation layer (or referred to as a tunneling insulation layer), a charge trap layer, and a blocking insulation layer. For example, the charge storage layer CS may have an oxide-nitride-oxide (ONO) structure. Also, a gate electrode GE including the selection lines GSL and SSL and the word lines WL**1** to WL**8** may be provided on an exposed surface of the charge storage layer CS and in a region between two adjacent common source lines CSL.

[0094] Drains or drain contacts DR may be respectively provided on the plurality of pillars P. For example, the drains or drain contacts DR may each include silicon on which impurities having the second conductive type are doped. The bit lines BL**1** to BL**3**, which extend in the second direction (for example, an X direction) and are arranged to be spaced apart from each other by a certain distance along the first direction may be provided on the drains DR.

[0095] U.S. Pat. Nos. 7,679,133, 8,553,466, 8,654,587 and 8,559,235 and U.S. Patent Application No. 2011/0233648 disclose appropriate elements of a three-dimensional (3D) memory array, which include a plurality of levels and in which word lines and/or bit lines are shared between the plurality of levels. In the present specification, the reference documents may be combined through citation.

[0096] FIG. **15** is a block diagram illustrating an example where the memory system according to an example embodiment is applied to a memory card system **600** For example, the memory system is assumed as a flash memory system.

[0097] Referring to FIG. **15**, the memory card system **600** may include at least a host **610** and a memory card **620**. The host **610** may include a host controller **611** and a host connector **612**. The memory card **620** may include a card connector **621**, a card controller **622**, and a memory system **623**, In an example embodiment, the memory system **623** may be implemented by using the example embodiments of FIGS. **1** to **13**. Therefore, the memory system **623** changes a command scheduling method to perform efficient garbage collection, based on the workload level according to the example embodiments.

[0098] The host **610** may write data in the memory card **620** and/or may read the data stored in the memory card **620**. The host controller **611** may transmit a command CMD, a clock signal CLK generated by a clock generator (not shown) included in the host **610**, and data DATA to the memory card **620** through the host connector **612**.

[0099] In response to a request received through the card connector **621**, the card controller **622** may supply data to the memory system **623** in synchronization with a clock signal generated by a clock generator (not shown) included in the card controller **622**. The memory system **623** may store data transmitted from the host **610**.

[0100] The memory card **620** may be implemented with a compact flash card (CFC), a Microdrive, a smart media card (SMC), a multimedia card (MMC), a security digital card (SDC), a universal flash storage device (UFS), a memory stick, an USB flash memory driver, and/or the like.

[0101] FIG. **16** is a block diagram illustrating an example where the memory system according to example embodiments is applied to an SSD system **700**.

[0102] Referring to FIG. **16**, the SSD system **700** may include a host **710** and an SSD **720**. The SSD **720** may transmit or receive a signal to or from the host **710** through a signal connector and may be supplied with power through a power connector. The SSD **720** may include an SSD controller **721**, an auxiliary power supply **722**, and a plurality of nonvolatile memory systems **723** to **725**. Each of the nonvolatile memory systems **723** to **725** may include the memory device according to the example embodiments. According to an example embodiment, therefore, each of the nonvolatile memory systems **723** to **725** changes a command scheduling method to perform efficient garbage collection, based on the workload level according to the example embodiments.

[0103] The memory controller **110**, the CMD scheduler **115***a*, the work load calculator **115***b*, the working memory **220**, the garbage collector **223**, the processor **210**, the control logic **320**, the workload calculator **400**, the valid page ratio calculator **420**, the non-free ratio calculator **440**, the command scheduler **500**, the CMU priority manager **520**, the CMD quota manager **540**, the host controller **611**, and the card controller **622** are either implemented using hardware components, a processor executing software components, or a combination thereof. Upon execution of one or more algorithms, described in example embodiments of inventive concepts, the aforementioned hardware components, or processor executing software components, result in a special purpose processor.

[0104] Algorithms, as presented in example embodiments of inventive concepts, constitutes sufficient structure, that may comprise of, including but not limited to, mathematical formulas, flow charts, computer codes, and/or necessary steps, which upon execution result in a special purpose computer that is programmed to perform the disclosed algorithms in example embodiments of inventive concepts.

[0105] It should be understood that example embodiments described herein should be considered in a descriptive sense